Real Time Digital Simulation and HIL Test of Xiamen MMC-HVDC Demonstration Project

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Abstract—**Xiamen MMC-HVDC demonstration project is the first real bipolar MMC-HVDC project in the world. Generally, before field commissioning of the project, the performance of control and protection system must be verified using hardware-in-the-loop (HIL) real time digital simulation. This paper presents the configuration and performance of a HIL test platform based on RT-LAB. Results from the HIL test platform and the field test are presented in this paper. By way of comparison between the results of HIL test and field test, the validity of RT–LAB HIL test platform is confirmed.**

***Index Terms*—MMC-HVDC, Hardware-in-the-loop (HIL), RT-LAB**

I. Introduction

Xiamen MMC-HVDC demonstration project is located in Xiamen City, China, which has been commissioned and put into operation on December 27th, 2015. The voltage rating of the project is ±320KV, and the power rating is 1000MW. This project is connected between the Pengcuo and Hubian stations. And it is a real bipolar MMC-HVDC project which has the highest voltage level and the largest power capacity till now. After putting it into service, the strength of the power grid in Xiamen has been raised, and the future demand of power in Xiamen can be satisfied. In addition, the reactive power can be adjusted rapidly, and the voltage stability and reliability of Xiamen power grid can be significantly enhanced.

As the real bipolar MMC-HVDC is an emerging and complex technology, the control and protection (C&P) scheme for this bipolar MMC-HVDC system is required to be test , before testing it with the real MMC converter together. HIL test is an effective method for the MMC test[1]. The period and cost of test can be reduced by HIL test as well as the C&P scheme can be tested in closed loop[2].

In this paper, RT-LAB real time simulation platform is introduced to simulate the main circuit of Xiamen MMC-HVDC project. The MMC valve is simulated in FPGA with a time-step of 250ns, and the rest of the main circuit is simulated in CPU with a time-step of 50us. The State-space Nodal (SSN) interface is used to couple the models simulated on FPGA and on CPU respectively. The whole HIL test platform is established by integrating the real C&P system to the RT-LAB platform using analog and digital IOs, as well as optical fiber communication interface. The validity of the proposed methodology for the C&P performance test is confirmed by comparing the results from the HIL test and the actual results from the field, after the project commissioning.

II. Control And Protection System Under Test

The single line diagram of Xiamen MMC-HVDC project is shown in Fig. 1 and Fig.2 . From the figures, it is clearly seen that each MMC Station consists of 2 MMC converters, namely the positive pole MMC converter and negative pole MMC converter respectively.

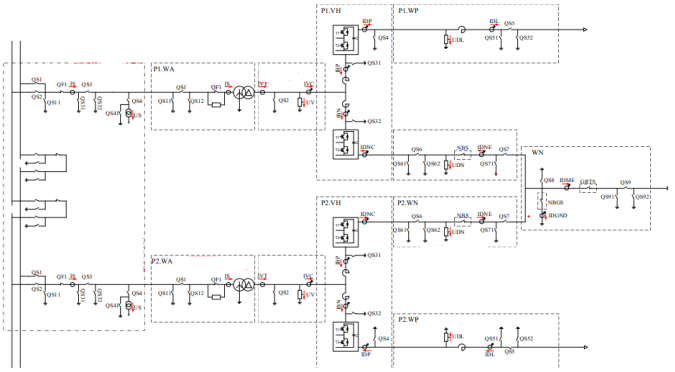

Fig. 1 Single line Diagram of Pengcuo MMC Station

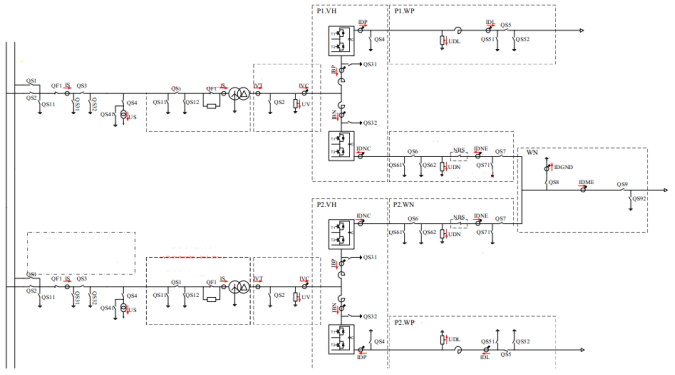

Fig. 2 Single line Diagram of Hubian MMC Station

As shown in Fig. 3, the C&P system for the Xiamen MMC-HVDC project is composed of four subsystems, including the system control center (SCC) , the pole control and protection (PCP), and the circulating current suppression controller (CCSC), and the voltage balancing controller (VBC), respectively.

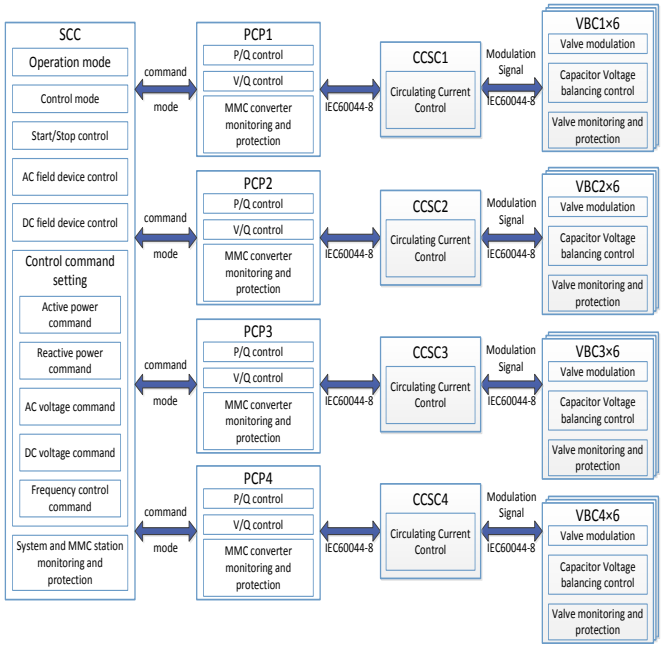

Fig. 3MMC control and protection system

The SCC controls the operating modes of the whole MMC-HVDC system, and monitors the status of the 2 MMC Stations. According to the operating mode, SCC sends the control command to the PCP, such as active and reactive power reference value, DC voltage reference value, etc. It also acquires the measurements of the electrical system, such as the system frequency, voltages and currents, power flow, etc.

There are 4 PCPs, each of them controls and protects one MMC converter. Thus, there are 2 PCPs in each station. PCP receives the command from SCC and selects the appropriate control mode according to the command. It sends 6 reference signals to the CCSC using optical fiber communication protocol IEC60044-8. Pole Protection scheme for the faults are also implemented on the PCP.

CCSC measures the arm current of the MMC converter and adopts suitable control algorithm to revise the reference signals received from the PCP, and then sends the revised reference signals to the VBC using optical fiber communication protocol IEC60044-8, thereby suppressing the circulating current of the arm current.

In the implementation of this HIL test bench, the VBC is simulated in the FPGA, and receives the revised reference signals from the CCSC and modulates the switching commands for each sub-module in MMC arm to balance the voltage of sub-modules within the arm.

III. HIL TEST BENCH

The HIL Test Bench is deployed using the RT-LAB real-time simulator. The RT-LAB real-time simulator simulates the AC and DC electrical circuits, including the MMC converters, and exchanges signals with the C&P under test in real-time.

A. Real-time Simulator

The RT-LAB real-time simulator uses the architecture which is comprised of off-the-shelf components. The simulation of the MMC Sub-modules is implemented in OP7020 which consists of Xilinx Virtex -7 FPGA under time step of 250ns, while the AC power grid is simulated on the OP5600 which is comprised of 2 Intel i7 6-core processors and a Xilinx Spartan-3 FPGA. The I/O modules and pins are physically integrated in the OP5600 through a carrier board. The I/O modules include analog modules and digital modules. The analog modules are used to send the analog signals including voltages and currents to the actual C&P system under test, and the digital modules are used to receive circuit breaker commands and send back the corresponding circuit breaker status[4]. The OP7020 can simulate up to 6000 MMC Sub-modules, as well as low level control including VBC and pulse generation in real time[5]. The OP7000 is a Virtex-6 FPGA-based simulator, which is used for the implementation of optical fiber communication protocol IEC60044-8. The Dolphin Switch is used for connecting the OP5600、OP7020 and OP7000 to exchange simulation data between them via PCI Express protocol. Fig.4 shows the configuration of the HIL test bench used in the Xiamen MMC-HVDC project.

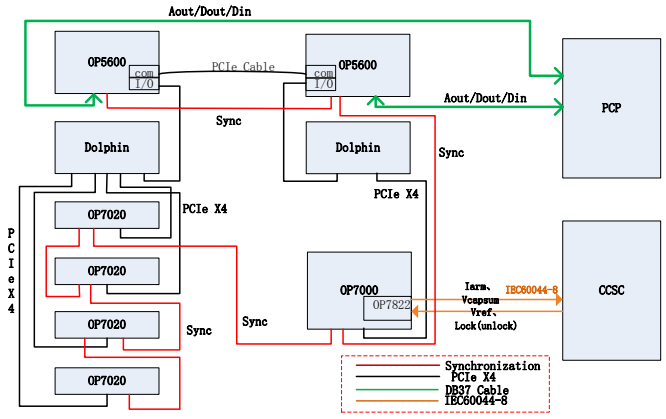

Fig. 4 Block Diagram of the HIL Test Bench

B. Real-time Simulation Model

The system parameters of each MMC station are given in table I.

TABLE I. Parameters of Xiamen MMC-HVDC Project

Parameters	Pengcuo Station	Hubian Station
Transformer connection	Y/D	Y/D
Rated Power(MVA)	1000MVA	1000MVA
Primary voltage(kV)	230kV	230kV
Secondary voltage(kV)	166.75kV	166.75kV
Arm Inductance(mH)	60mH	60mH
DC inductance(mH)	50mH	50mH
Number of SMs per arm	216(including 16 redundant SMs)	216(including 16 redundant SMs)
Sub-module capacitance(F)	0.01F	0.01F

The real-time simulation model of Xiamen MMC-HVDC demonstration project is established using MATLAB/Simulink. The modules including power sources and passive components (resistors, inductors, and capacitors) are from SimPowerSystem (SPS) library in MATLAB/Simulink, which are solved using the state-space approach. The wide-band line module used to simulate the DC transmission cable and On-load Tap-Changing (OLTC) transformer module are developed using the classic nodal approach. The mathematical model of MMC valve is

presented in [5], and the VBC and pulse generation algorithm is presented in [3].

As in [5], the Sub-module (SM) can be replaced by a equivalent circuit, as shown in Fig.5. For all operation modes of SM, including Insertion, Bypass, Diode, and Fault mode, Vsp and Vsn can be represented in TABLE II. The s1 and s2 are the upper and lower IGBT status of SM, respectively, where value 1 represents on-state and 0 represents off-state.

TABLE II. Source voltages in SM equivalent circiuit

Mode	s1	s2	*Vsp*	*Vsn*
Insertion	1	0	V_c+ V_{fd}	V_c -V_{fk}
Bypass	0	1	V_{fk}	-V_{fd}
Diode	0	0	V_c+ V_{fd}	-V_{fd}
Fault	1	0	V_{fk}	-V_{fk}

Vfd and Vfk are the diode and IGBT forward conduction voltages, and Vc is the capacitor voltage.

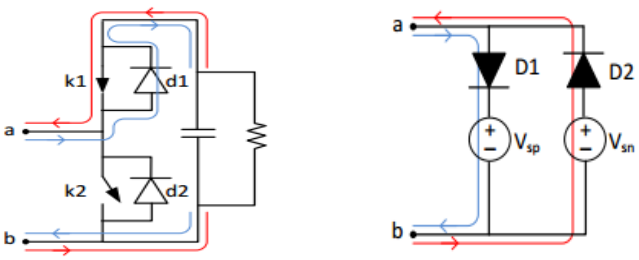

Fig.5. A general SM equivalent circuit

By analyzing the circuit above, the equation to calculate the capacitor voltage is derived as below,

$$V_c = \frac{1}{C_{SM}}\int i_c d_t = \frac{1}{C_{SM}}\int (s \cdot i_{val} - \frac{V_c}{R_{disc}})d_t \qquad (1)$$

In (1), Vc is the capacitor voltage; ic is the capacitor current; C_{SM} is the SM capacitance; i_{val} is the arm current; R_{disc} is the discharge resistance; *s* is a variable determined by the IGBT status and the arm current direction, as shown in TABLE III. The positive arm current direction is specified as the current flows from terminal-a to terminal-b.

TABLE III. Parameter *s* in Capacitor Voltage Equation

Mode	s1	s2	Arm current direction	*s*
Insertion	1	0	either	1
Bypass	0	1	either	0
Diode	0	0	positive	1
			negative	0

Since the MMC arm is comprised of multiple serially connected SMs, so the arm equivalent circuit consists of serially connected SM equivalent circuits shown in Fig. 6(a). Because the series connection of diodes can be equivalent as one diode and the multiple voltage sources behind the diode can be represented by one voltage source, the arm equivalent circuit can be further equivalent to 2 controllable voltage sources behind two diodes, as in Fig. 6(b). Each source voltage value, *Vsx*Σ, is the summation of the individual SM source voltages, Vsx-i, where x represents either p or n, and N represents the number of SM in an arm.

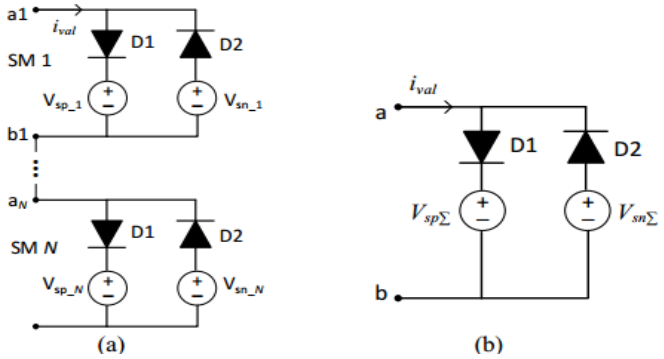

Fig.6. Equivalent circuits of (a) a stack of SM and (b) MMC arm

RT-LAB develops an unique solver which is State-space nodal (SSN)[6]method, it can naturally couple the model based on state-space approach and model based on classic nodal approach together. In fact, SSN is used to split the whole model into a few SSN groups. Fig.7 shows how a MMC converter is splited into a few SSN groups.

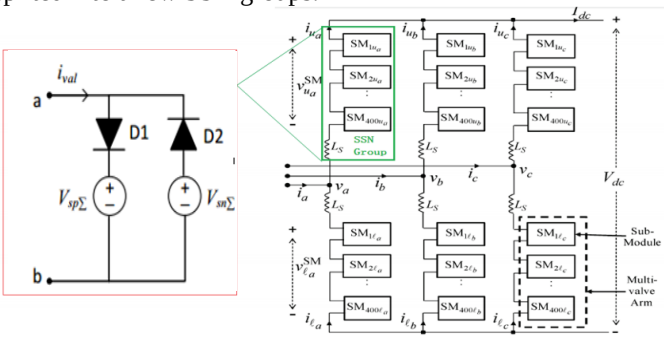

Fig.7. Equivalent circuit of MMC valve

Each SSN group is computed using 5th order solver which is called Artemis. For better stability, Artemis adopts Backward-Euler method to solve the Artemis equations to suppress numerical oscillations while discontinuities emerge[7].

The SSN method allows parallel computation of each MMC valve in the same time without artificial delays. This will improve the simulation speed and accuracy for real-time simulations[8].

IV. Performance Test

Performance test of the complete C&P system is necessary to evaluate its function in various operation scenarios. More than hundreds of scenarios have been tested. Due to the limitation by the length of this paper, only a few typical test scenarios are demonstrated below.

A. MMC deblocking test

After the DC bus voltage is charged to about 0.7pu by the sending end MMC station, which controls the DC bus voltage, the controller will then deblock the sending end MMC station to control the DC bus voltge to about 0.9375pu instead of 1pu and hence reduce the overcurrent. After the DC bus voltage is stable at about 0.9375pu, then deblock the receiving end MMC station, and then control the DC bus to 1pu. The HIL test results of deblocking the sending end MMC station are present in Fig.7, and are compared with the field test results shown in Fig.8.

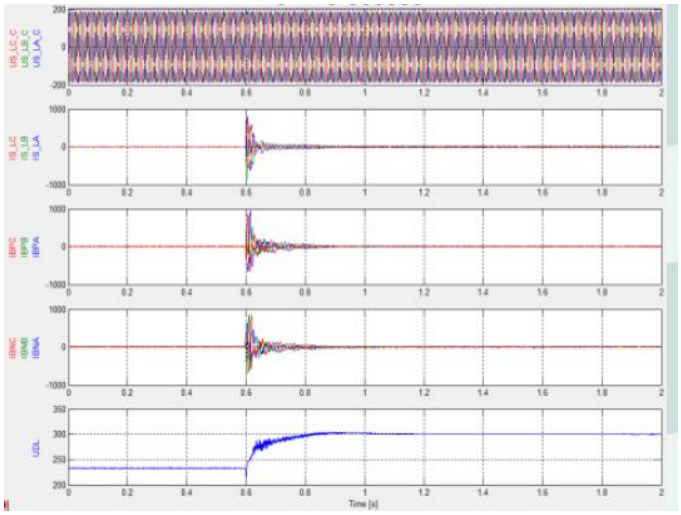

Fig.7. HIL test results of deblocking the sending end MMC valve

In Fig.7, the first graph is the grid side AC voltage, the second graph is the AC side current, the third graph is the 3 –phase upper arm current of positive pole MMC valve of sending end MMC station which control the DC bus voltage, the fourth graph is the 3–phase lower arm current of negative pole MMC valve of sending end MMC station, the last graph is the DC bus voltage.

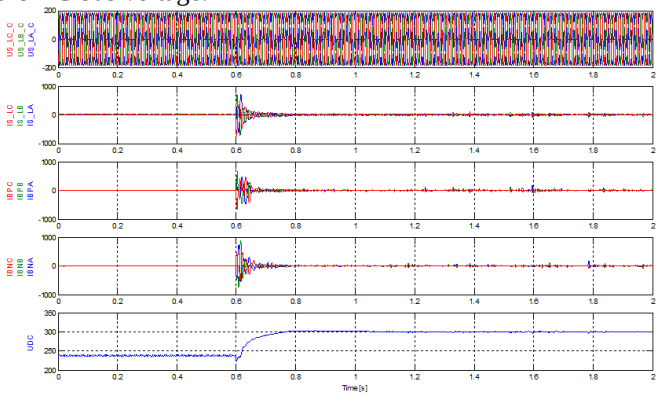

Fig.8. Field test results of deblocking the sending end MMC valve

In Fig.8, the measured quantities displayed in this figure is same as Fig.7. The test results in Fig.7 are very similar to those obtained in Fig.8. The comparison proves that the HIL test is able to reflect the dynamic response in the field.

B. Power control test

After the DC bus voltage is controlled to 1pu, and the 2 terminal MMC–HVDC enter into normal operation mode. During normal operation mode, power control test is implemented.

Fig.9 presents the HIL test results of power control. In Fig.9, the first graph is the grid side 3-phase AC voltage, the second graph is the grid side 3-phase AC currents, the third graph is the DC bus voltage, and the fourth graph is the active power, and the last graph is the reactive power.

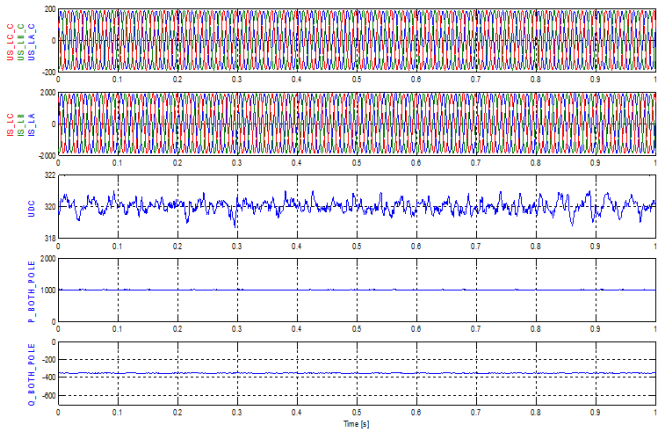

Fig.9. HIL test results of power control

From fig.9, it is shown that the active power is controlled at 1000MW, the reactive power is controlled at -350Mvar, and the DC bus voltage is stable at 320kV.

Fig.10 and fig.11 present the field test results of the power control test during field commissioning period. The measured quantities displayed in fig.10 are same as the first 4 quantities displayed in fig.9. The first 3 quantities displayed in fig.11 are same as the first 3 quantities displayed in fig.9, the last quantity displayed in fig.11 is reactive power.

From fig.10, it is shown that the active power is controlled at 200MW, and the DC bus voltage is stable at 320kV.

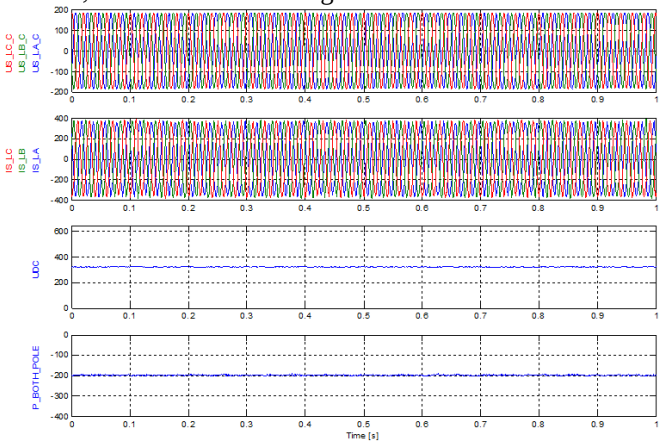

Fig.10. Field test results of active power control

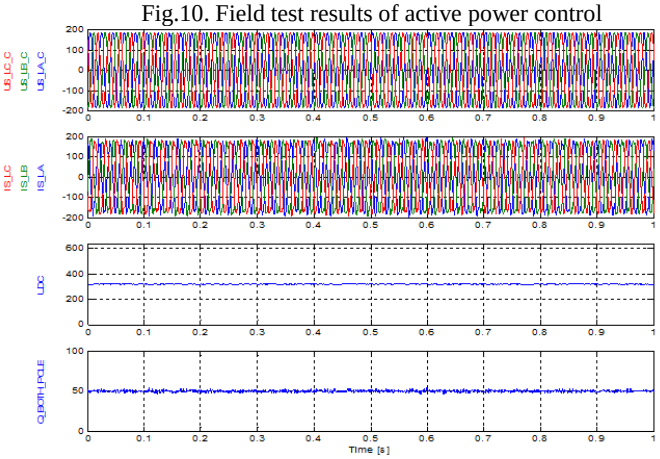

Fig.11. Field test results of reactive power control

From fig.10 and fig.11, it is shown that the active power is controlled at 200MW, the reactive power is controlled at 50Mvar, and the DC bus voltage is stable at 320kV.

By comparison between the HIL test results and field test results of power control, it proves that C&P system works well, and the HIL test results can validate the real performance of C&P system in the field commissioning.

V. CONCLUSION

This paper presents the HIL test for the performance of Xiamen MMC-HVDC demonstration project. An overall HIL test architecture is presented, and the HIL test results obtained from the HIL test has been compared with the field test results during field commissioning. The comparison proves that the HIL test is a effective approach to verify the performance of the whole Xiamen MMC-HVDC system.

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