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Modeling and Real-time Simulation of Modular Multilevel Converters using RT-LAB

Mingyang Wei, Deyou Wang, Guangye Liu
Shanghai KeLiang Information Tech. & Eng. Co., Ltd

***Abstract*—Modular Multilevel Converter (MMC) is composed by hundreds of sub-modules (SMs). Such a large scale power electronic switches and power nodes will become very difficult to solve in the process of real-time simulation of the electromagnetic transient. These switches will occupy a very large amount of calculation, in this case, still use a large step (microsecond) simulation has been unable to meet the sub-module operation during dynamic response, especially when a short circuit fault occurs in the bridge arm, the electromagnetic transient process of the system cannot be accurately reflected. In order to solve the problem, this paper presents a simplified sub-module model and an equivalent valve model based on state-space node solver implemented in FPGA for the real-time simulation. This method can effectively reduce the power nodes and decrease the computation time, and improves the accuracy of the simulation. In addition, the multi-rate simulation of RT-LAB and the test method of hardware-in-the-loop (HIL) are explained in this paper. Finally the simulation results show that the effectiveness of the proposed method.**

***Index Terms*—Modular Multilevel Converter; Real-time simulation; State-space Nodal Solver; Hardware in the loop.**

I. INTRODUCTION

The flexible high-voltage direct current transmission (HVDC) is based on voltage source converter, compared with the traditional two-level and three-level inverters, MMC based on the structure of modular multilevel converter has greater advantages: MMC's loss is less due to the low switching frequency. Because of the MMC's output voltage harmonic content is low, so the ac filters can be dispensed with, and cost savings. By changing the number of sub-modules in each phase can easily increase the voltage level [1-4].

Although the HVDC transmission based on MMC has many advantages, but, in the process of electromagnetic transient real-time simulation, too much power switches can cause a lot of calculation difficulties, the reason is that a great deal of the nonlinear components in the inverter through iteration to solve the global matrix during the period of operation, and greatly increased the burden of the simulation. So, for a real-time simulation system, accurately simulate a switch beyond the existing simulation technology ability, we need to use some simplified approaches to implement network integration and study the simulation technology on hardware in the loop.

This paper firstly to simplify the IGBT and fly-wheel diode into a switchable element R_{on} and R_{off}, and each SM capacitor is replaced by an equivalent current history source in parallel with a resistance. Using the large and small resistance to simulate real IGBT switching actions can significantly reduce the simulation burden. But the shortcoming of this approach is that, when the number of SM are increased, the simulation losses and the loop current between the bridge arms are bigger than the actual working condition, and the charging waveforms are not accurate. In order to solve this problem, the FPGA chip implemented in the real-time simulation platform with a less than 1 millisecond step size, by using time-sharing multiplexing technology to calculate a large number of SMs, and ensure that the simulation precision of the voltage source inverter. On the other hand, the simulation step size are different between the model of MMC valve running on the FPGA chip and the model of ac/dc running on the CPU, and the CPU and FPGA still exist synchronization and delay problems in the process of exchange data, these problems are inevitable due to the synchronous parallel computation on different hardware. The classic real-time simulation algorithms using the natural transmission delay of circuit (such as dozens of kilometers of cable) to decouple circuit on different hardware chips, but in the flexible HVDC system, especially in the back to back HVDC system has some limitations by using cable decoupling [5]. In order to solve the problem, this paper uses the state space nodes method to decouple the ac and dc grid, it can meet various working conditions of the flexible HVDC system real-time simulation. The method was introduced in detail in this paper, and the simulation results show that the effectiveness of the proposed method.

II. MMC MODELING

A. MMC Topology and Operation Principle

Three-phase modular multilevel converter topology is shown in Fig.1, the converter has six bridge arm, each arm is composed of a reactor and N SMs in series, the upper and lower bridge legs together referred to as a unit.

SM adopts a half bridge structure, when the upper gate of an SM is ON, the SM output voltage equals its capacitor voltage and the SM is considered as an ON SM. When the lower gate of an SM is ON, the SM outputs 0 voltage and it is considered as an OFF SM. Each bridge arm voltage can be equivalent to a controlled voltage source, under the normal operation of the dc voltage remains unchanged. As shown in Fig.1, the number of devoted SMs is the same in each unit. In the normal process of operation, the SM's capacitor voltage is controlled by its nominal value. Then, the total per-unitized voltage of all SM in one arm is equal to the number of ON SM. Therefore, MMC is considered as a VSC and it can be represented by a controllable voltage source[6].

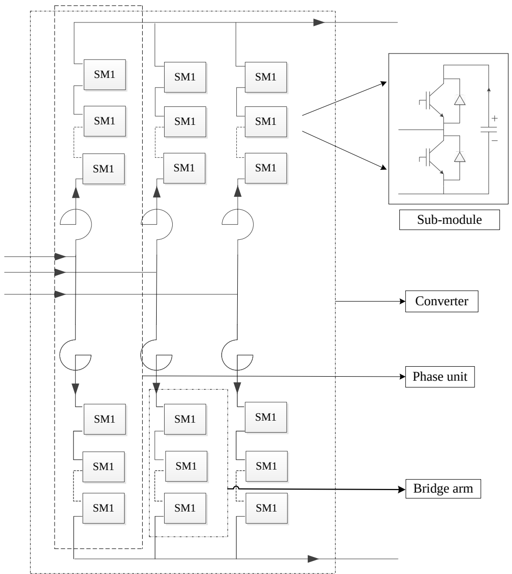
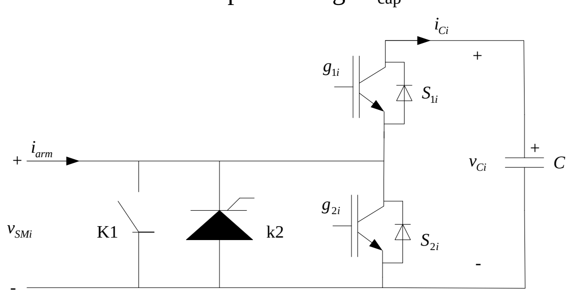


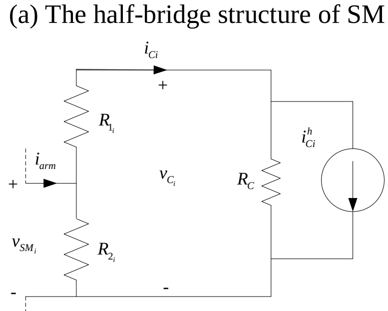
Fig.1 MMC topology

B. *MMC Modeling*

The half-bridge structure of SM is shown in Fig. 2(a). Just like real SM, it uses a high-speed bypass switch K1 to simulate the function of SM bypass removal, in order to reflect the safety and reliability of MMC valve, and it also uses a thyristor K2 for fault current stream to protect IGBT. Two IGBT devices of each SM are controlled by two gate signals, and according to the conduction state it outputs voltage v_{cap} or 0.



(a) The half-bridge structure of SM



(b) The equivalent circuit of SM

Fig.2 the detailed and simplified model of single SM

In this paper, the SM power switches are replaced by ON/OFF resistors: R_{ON} (milliohm) and R_{OFF} (megohm). This approach allows performing an arm circuit reduction for eliminating internal electrical nodes and allowing the creation of a Norton equivalent for each MMC arm. In Fig.2(b), R_1 and R_2 are controlled and used for replacing the two IGBT/diode combinations. With the trapezoidal integration rule, each SM capacitor is replaced by an equivalent current history source $i_{C_i}^h(t-\Delta t)$ in parallel with a resistance $R_C = \Delta t/(2C)$ [7], where Δt is the numerical integration time-step.

C. *SSN-MMC Model*

The approach presented above derives the Norton equivalent circuit of each MMC arm using nodal equations. In the Simulink/SimPowerSystems environment, based on state-space equations, the same discretized Norton equivalent circuit can be derived with the ARTEMIS State-Space Nodal(SSN) solver used in RT-LAB[8-10].

Considering the state-space equations of a generic circuit

$$\begin{cases} \dot{x} = A_K x + B_K u \\ y = C_K x + D_K u \end{cases} \tag{1}$$

Where x and u are the state variable and input vectors respectively (they can be either current or voltage variables).

The discretization of equation (1) can be derived

$$\begin{cases} x_{t+\Delta t} = \hat{A}_K x_t + \hat{B}_K u_t + \hat{B}_K u_{t+\Delta t} \\ y_{t+\Delta t} = C_K x_{t+\Delta t} + D_K u_{t+\Delta t} \end{cases} \tag{2}$$

Where Δt is the integration time-step and the hated matrices result from the discretization process.

By combining and reorganizing equation (2)

$$y_{t+\Delta t} = C_K[\hat{A}_K x_t + \hat{B}_K u_t] + [C_K \hat{B}_K + D_K]u_{t+\Delta t} \tag{3}$$

It is apparent that the above equation has an historic term and can be rewritten as

$$y_{t+\Delta t} = y_{hist} + W_K u_{t+\Delta t} \tag{4}$$

If the input $u_{t+\Delta t}$ is a voltage variable, then W_K is an impedance, y_{hist} and $y_{t+\Delta t}$ are currents variables equation (4) is therefore the Norton equivalent of the generic circuit.

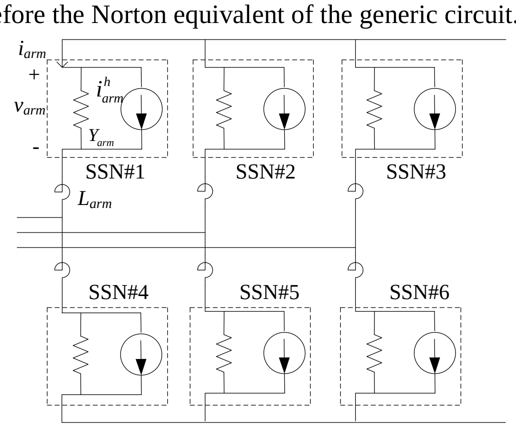


Fig.3 The MMC valve model based on SSN

MATLAB/Simpower System model is decomposed into formula (1) in the form of different branch or combination, SSN solver automatically get NORTON equivalent circuit or thevenin's equivalent circuit, and at the same time with a classic node admittance method to solve. SSN solver can be embedded artificial coding procedures, such as the MMC bridge arm highly repetitive topology, six bridge arm can be divided into six parts, the same artificial coded program in FPGA to calculate. As shown in figure 1 of the six bridge arm of MMC decoupling and respectively based on SSN solver code calculation, SSN - MMC model as shown in Fig.3.

The following steps(including also the BLOCKED state) and the main equations of the algorithm implemented in Matlab/Simulink are presented in Fig.4.

The algorithm considers each SM separately and maintains a record of each capacitor voltage and current. It is applicable to any number of SMs per arm.

Real-time simulation requires fast computations. Precomputation and optimization of the code is necessary to improve computational speed without effecting model accuracy. In the MMC code, each SM can have three circuit configurations depending on the states: ON, OFF and BLOCKED. Thus, in step 4, the equivalent Thevenin resistance of each SM (R_{SM_i}) and the resistive term that allows computing the Thevenin voltages ($v^h_{SM_i}$), are pre-computed since they can only have three different values.

In point Fig. 4.2, the ON/OFF states can be computed directly according to gate signals. However, the BLOCKED state is defined depending on state and non-state variables. Thus, the zero-crossing of the arm current variable will cause numerical oscillations. To avoid this problem, the implementation of an iterative process could be a solution; however this approach will require more computing time which is problematic for real-time performance. In order to overcome this issue, a trigger is added to detect and maintain the "High impedance mode" (Fig. 4.2) for one more time-step. Each SSN group (or decoupled circuit) uses a 5^{th} order solver to compute its Norton equivalent circuit, for better precision and the Backward-Euler solver is used to solve the global network circuit to eliminate numerical oscillations when discontinuities occur.

1) Retrieve arm voltage from the network solution and compute arm current:

$$i_{arm}(t) = v_{arm}(t).Y_{arm}(t-\Delta t) + i^h_{arm}(t-\Delta t)$$

2) For each SM, set R_1 and R_2 values depending on gating signals, current arm direction, previous SM voltage and previous capacitor voltage:

$if\,(SM_i = ON\_state)$
$\{\, R_{1i} = R_{ON}\,;\, R_{2i} = R_{OFF} \,\}$
$elseif(\, SM_i = OFF\_state\,)$
$\{\, R_{1i} = R_{OFF}\,;\, R_{2i} = R_{ON} \,\}$
$elseif(\, SM_i = BLOCKED\_state\,)\{$
$if((\, i_{arm}(t) > 0\,)\&\&(\, v_{SMi}(t\text{-}\Delta t) > v_{Ci}(t\text{-}\Delta t)\,))$
$\{\, R_{1i} = R_{ON}\,;\, R_{2i} = R_{OFF} \,\}$
$If((\, i_{arm}(t) < 0\,)\&\&(\, v_{SMi}(t\text{-}\Delta t) < 0\,))$
$\{\, R_{1i} = R_{OFF}\,;\, R_{2i} = R_{ON} \,\}$
$Else$
$\{\, R_{1i} = R_{OFF}\,;\, R_{2i} = R_{OFF} \,\}\}$

3) Compute capacitor voltages and currents for each SM:

$$i_{Ci}(t) = i_{arm}(t) - \frac{v_{R_{2i}}}{R_{2i}}\,;\, v_{Ci}(t) = (i_{Ci}(t) - i^h_{Ci}(t))R_C$$

4) Compute Thevenin equivalent for each SM:

$$R_{SMi(t)} = \frac{R_{2i}(R_C + R_{1i})}{R_{2i} + R_{1i} + R_C}$$

$$v^h_{SMi}(t-\Delta t) = R_{SMi}(t)\left(\frac{R_C}{R_C + R_{2i}}\right) i^h_{Ci}(t-\Delta t)$$

5) Compute voltages of each SM:

$$v_{SMi}(t) = i_{arm}(t)R_{SMi}(t) + v^h_{SMi}(t-\Delta t)$$

6) Compute and send Norton equivalent(Fig.3):

$$Y_{arm}(t) = \frac{1}{\sum_{i-1}^{N} R_{SMi}(t)}$$

$$v^h_{arm}(t-\Delta t) = \sum_{i=1}^{N} v^h_{SMi}(t-\Delta t)$$

$$i^h_{arm}(t-\Delta t) = -v^h_{arm}(t-\Delta t)Y_{arm}(t)$$

Fig .4 SSN-MMC arm algorithm

III. MMC REAL-TIME SIMULATION BASED ON RT-LAB

RT-LAB real-time simulation system was developed by Canadian OPAL-RT technologies, it is the world leader in the development of PC/FPGA based real-time digital simulators, Hardware in the Loop (HIL) testing equipment and Rapid Control Prototyping (RCP) systems. The simulation system based on the high performance computer equipped with high-end CPU processor and FPGA architecture of the shelves, it has a strong capacity and flexible extension function.

A. Multi-rate simulation

The model of MMC-HVDC real-time simulation is composed of two parts, their operating rate are not the same and decoupled from each other. The SM is modeled in FPGA, and using the simulation step size of 500 ns, and other parts, including ac grid, the converter transformer, the bridge arm reactor, dc cable, as well as the circuit breaker, are simulated in the CPU with 20 to 50 us step size. According to the analysis above, MMC output voltage of each bridge arm is equal to the sum of all SM outputting voltage, so the MMC can be equivalent to a controlled voltage source, connecting with the ac side and dc side.

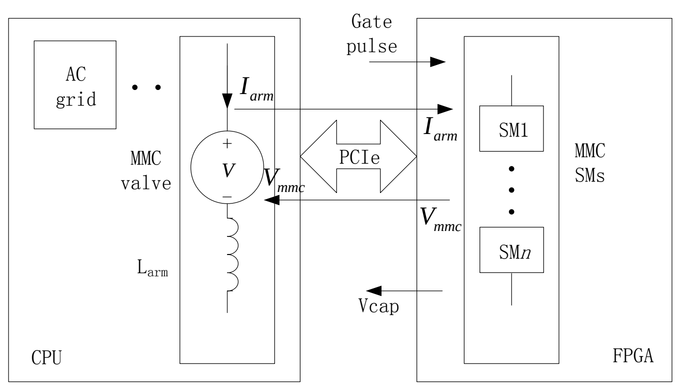


Fig.5 MMC-HVDC multi-rate simulation principle

Although the updating speed of SM in the FPGA is faster than the updating speed of ac grid in the CPU, but within a CPU sampling step they can synchronous interaction data. As shown in Fig.5, through a high-speed communications PCIe bus, the MMC voltage V_{mmc} can be sent from FPGA to the CPU, as the controlled voltage source control signal, while the bridge arm current I_{arm} can be sent from CPU to the FPGA and participate in the calculation.

Within a CPU simulation step the bridge arm current is changing slowly due to inhibition of bridge arm inductance, and from a slow system (CPU) passed into a rapid system (FPGA). As a result, the bridge arm current instantaneous value is sent to the FPGA and kept a CPU step time at the synchronization time point, until the arrival of the next synchronization time point, accordingly, the MMC voltage V_{mmc} quickly update in the FPGA, if the instantaneous value V_{mmc} at synchronization time point is sent to the CPU may cause errors in the model, it is because that the V_{mmc} may be a bad signal at the moment. So, in a CPU simulation step there is an average V_{mmc} is calculated and sent from the FPGA to the CPU model, thus effectively improve the simulation accuracy.

B. The hardware in the loop simulation

Hardware in the loop simulation is refers to the ac/dc power grid and MMC valve are virtual model in the flexible HVDC system, it is running in the real-time simulator. As mentioned above the multi-rate simulation, the control and protection equipment are the real system, through the IO and optical fiber connection between them, thus forming a closed loop system, as shown in Fig. 6. RT-LAB real-time simulation platform, which can simulate all kinds of steady state and transient operating conditions of the flexible HVDC system in real-time. At present, the control and protection equipment of flexible HVDC project before delivery of functional tests are done on RT-LAB platform in china, which greatly shorten the development and evaluation cycles of the control protection system, and promote the development of practical engineering.

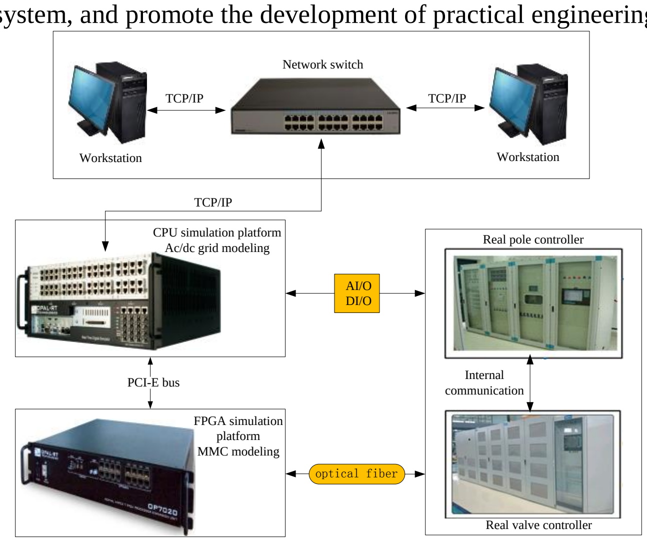


Fig. 6 HIL simulation test system based on RT-LAB

IV. SIMULATION VERIFICATION

The test results of the simulation are based on the actual engineering background. Using the above mentioned equivalent method, the MMC-HVDC simulation model is established, the main circuit of MMC-HVDC model is shown in Fig. 7. This is a back to back MMC-HVDC transmission system, and there is no dc cable.

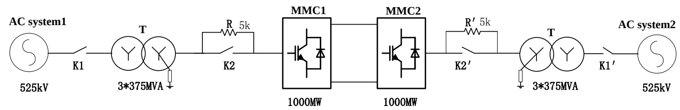


Fig. 7 MMC-HVDC transmission test system

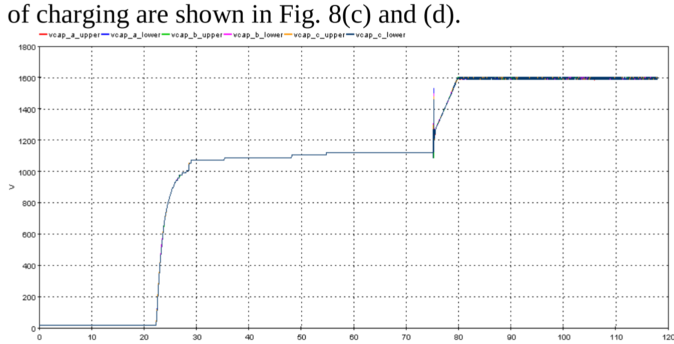
Tab 1 The parameters of MMC-HVDC system

Description of Parameters	Value
Grid voltage and frequency	525kV, 50Hz
Transformer power rating	1125MVA
Transformer ratio	525kV/375kV
Transformer impedance	14%
Arm Impedance	105mH
MMC power rating	1000MVA
Number of SM per arm in MMC1	335
Number of SM per arm in MMC2	438
SM capacitance	8mF
DC bus voltage	±350kV

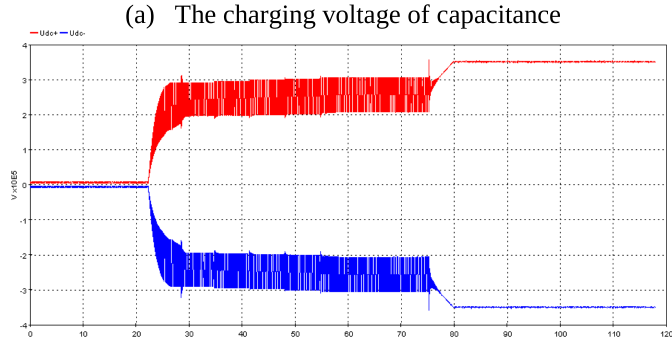
A. The charging process simulation of MMC-HVDC system

First, the start charging process of MMC2 station is simulated in this paper, as shown in Fig. 8. The whole process can be described as follow, after ac circuit breaker closed, the capacitance of SMs start charging, and the charging resistance in series in the circuit at the same time. After the stable operation, the bypass switch is closed, in the same time the charging resistance is bypassed, and start to charge for the second time. Until the dc side voltage rises to a certain value, the SMs begin to receive the pulse signal, and to track modulation wave in turn into or removal, the capacitance voltage rise to 1600V as shown in Fig. 8(a).

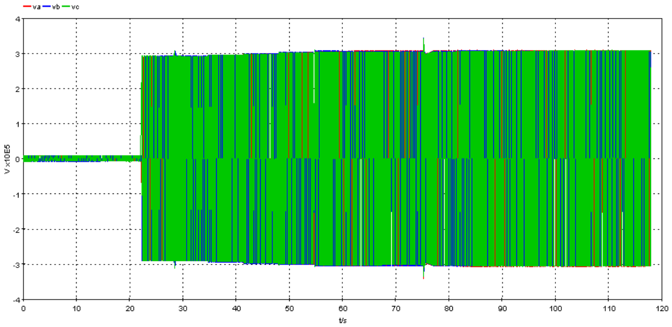
The charging process of dc side is shown Fig. 8(b), it also has two times charging process, and finally the dc voltage value rise to ±350kV. The voltage and current waveforms in the process of charging are shown in Fig. 8(c) and (d).



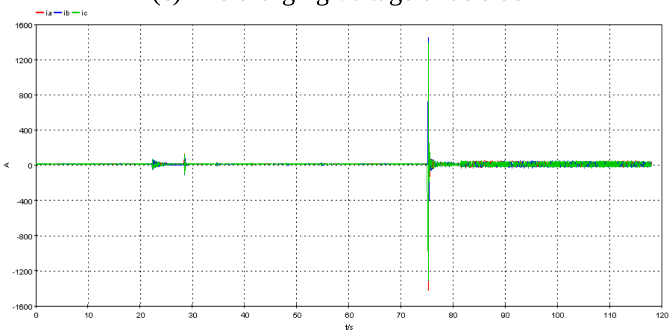
(a) The charging voltage of capacitance



(b) The charging process of dc side



(c) The charging voltage of ac side

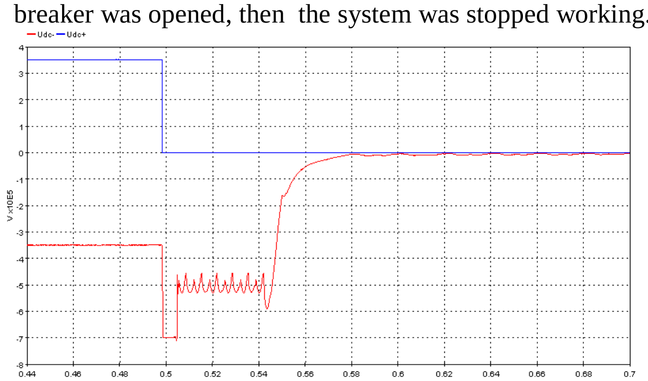


(d) The charging current of ac side

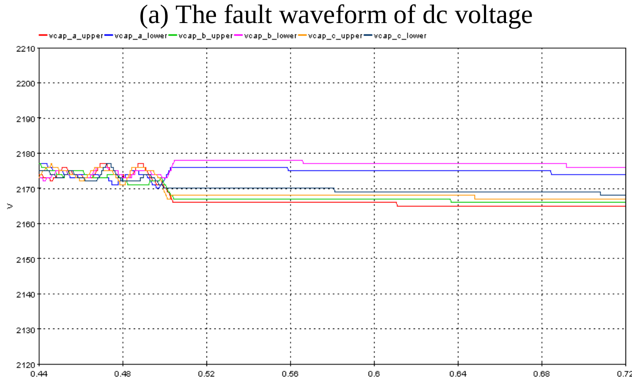
Fig.8 The charging waveforms of MMC2 station

B. The transient process simulation of MMC-HVDC system

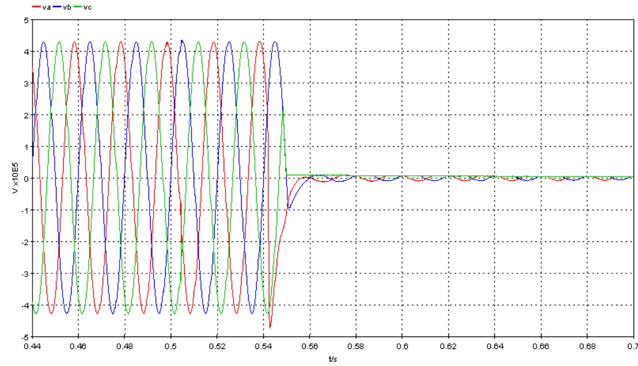
Under the HVDC running method, 10MW active power was transferred from MMC2 to MMC1. the real-time simulation waveforms of the positive pole to ground fault in dc side of MMC1 station are shown in Fig. 9. As shown in Fig.9(a), when the positive of the dc side to ground fault , the negative voltage rise rapidly for twice than before. 6ms later, the MMC1 valves were blocked, and 42ms later, the ac breaker was opened, then the system was stopped working.



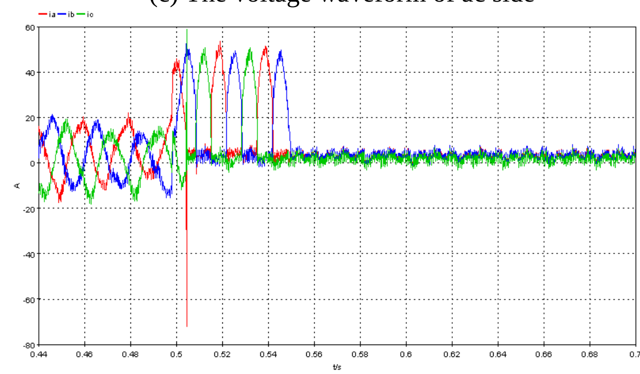
(a) The fault waveform of dc voltage



(b) The fault waveform of capacitance voltage



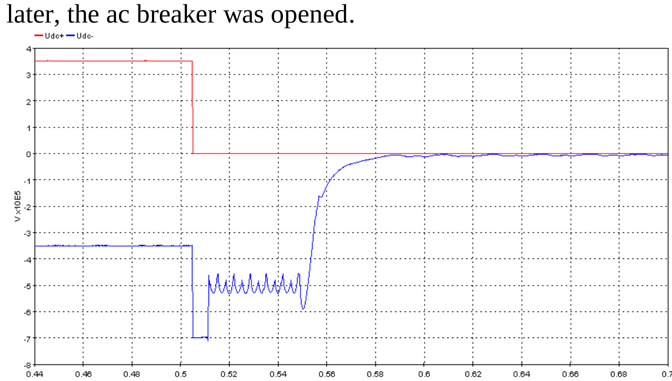
(c) The voltage waveform of ac side



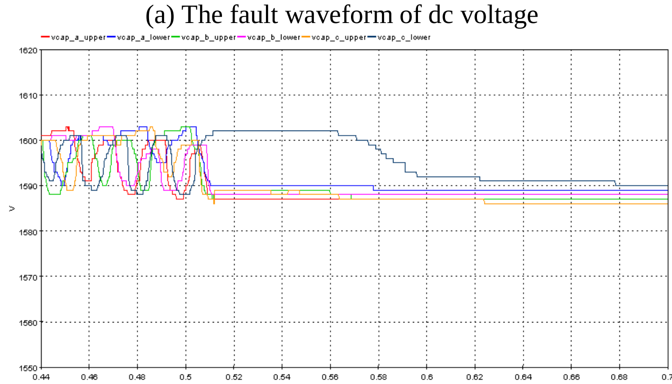
(d) The current waveform of ac side

Fig.9 The dc fault waveforms of MMC1 station

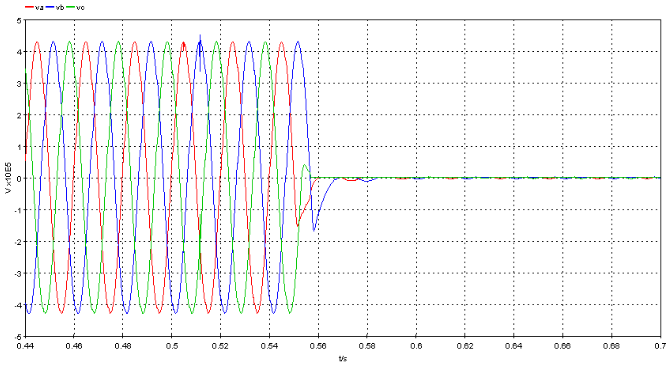
The real-time simulation waveforms of MMC2 station are shown in Fig. 10. It is similar to MMC1 station, the negative dc voltage rise rapidly for twice than before. The average voltage of SMs per bridge arm was changing nearby 1600V. 6ms later, the MMC2 valves were blocked, as shown in Fig. 10(a). The ac voltage waveform is shown in Fig. 10(c), this shows that 42ms later, the ac breaker was opened.



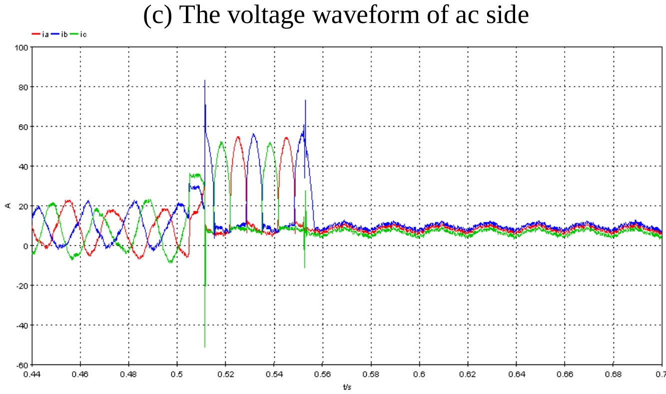
(a) The fault waveform of dc voltage



(b) The fault waveform of capacitance voltage



(c) The voltage waveform of ac side



(d) The current waveform of ac side

Fig.10 The dc fault waveforms of MMC2 station

V. Conclusions

The detailed model of SM is simplified as an equivalent model in this paper, it can effectively reduce the burden of real-time simulation. On the basis of the simplified model, The traditional model of the MMC valve automatically be equivalent to thevenin's equivalent circuit by SSN solver, this method can significantly improve the calculation speed and accuracy of real-time simulation, and it provides a reliable test platform for the engineering test and research.

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Mingyang Wei was born in Henan, China, in 1986. He received the B.Sc. degree in electrical engineering from the Henan polytechnic university, Henan, in 2009 and the M.A.Sc. degree in power electronics and power drives from Jiangsu university, Jiangsu, china, in 2012. From 2013 to now he worked at Keliang (Shanghai) on research and development activities related to the simulation and analysis of electromagnetic transients.

Deyou Wang was born in Anhui, China, in 1986. He received the B.Sc. degree in electrical engineering from the Hebei university of science and technology, Hebei, in 2010 and the M.A.Sc. degree in electrical theory and new technology from Fuzhou university, Fuzhou, china, in 2013. From 2014 to now he worked at Keliang (Shanghai) on research and development activities related to the simulation and analysis of electromagnetic transients.

Guangye Liu was born in Shandong, China, in 1987. He received the B.Sc. degree in electrical engineering from the Shandong polytechnic university, Shandong, in 2011 and the M.A.Sc. degree in power electronics and power drives from Liaoning university of science and technology, Liaoning, china, in 2014. From 2015 to now he worked at Keliang (Shanghai) on research and development activities related to the simulation and analysis of electromagnetic transients.

Contact Information

Mingyang Wei is with the Shanghai KeLiang Information Tech. & Eng. Co., Ltd, Number 829, Yishan Road, Shanghai, CHINA(phone number: +86-187-0181-6369, fax number: +86-21-5423-4721, e-mail: mingyang.wei@ keliangtek.com).